REMARKS

This is a full and timely response to the outstanding Office action dated October 23, 2007. Reconsideration and allowance of the application and all pending claims 1-2, 4-6, and 8 are respectfully requested.

Present Status of Patent Application

Upon entry of the proposed amendments in this response, claims 1-2, 4-6, and 8 remain pending in the present application.

Applicant has noted with great appreciation that claims 4, 5, and 8 remain allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Pertaining to the prior art rejection, claims 1-3 and 6-7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (USPN 4,772,833; hereinafter "Tanaka"). In response thereto, claims 1, 4, 6, and 8 have been amended for patently defining the invention over the cited reference. Specifically, the allowable subject matters in claims 3 and 7 have been encompassed into their respective independent claims 1 and 6, and claims 3 and 7 have been correspondingly canceled. It is believed that the foregoing amendments introduce no new matter to the present application and are fully supported by the written disclosure of the instant application. Reconsideration of the application as currently amended and based on the arguments set forth hereinbelow is earnestly solicited.

Response to Claim Rejections Under 35 U.S.C. Section 102(b)

Claims 1-3 and 6-7 stand rejected under 35 U.S.C. 102(b) as being anticipated by

Tanaka.

With respect to claim 1 of the present invention, as current amended, it recites the following:

"A circuit for performing pulse width modulation suitable for generating a PWM signal according to an input data with M+N bits , the pulse width of the PWM signal dithering in 2^N frames and corresponding to a value of the input data, comprising:

a pulse density modulator (PDM), for receiving the least N bits of the input data and generating a pulse density modulation signal, wherein a number of pulse of the pulse density modulation signal in 2^N frames correspond to a value of the least N bits of the input data;

a first adder, electrically coupled to the PDM for generating a PWM data by adding the most M bits of the input data to a value of the pulse density modulation signal; and

a pulse width modulator, electrically coupled to the first adder for generating a PWM signal dithering in 2^N frames according to the PWM data,

wherein **before a value of the most M bits of the input data is added to the value of the pulse density modulation signal by the first adder, the M bits input data is sign-extended to an input data with at least M+1 bits, so as to generate the PWM data with at least M+1 bits.**" (Emphasis added)

As indicated in Applicant's claim 1, before the first adder adds a value of the most M bits of the input data to the value of the pulse density modulation signal, the M bits input data is sign-extended to an input data with at least M+1 bits, such that at least M+1 bits PWM data are generated. Nevertheless, **the adder 52 taught by Tanaka is neither equipped with the function of sign-extending the signed bit nor able to prevent**

errors from occurring in the input data because of a data overflow.

In detail, as recited in paragraph [0031] of Applicant's specification, since the input data D[11:0] has a signed value, and D[11] is a signed bit, if the input data D[11:2] fed into the adder 220 is "01,1111,1111", and the pulse density modulation signal PDM generated by the adder 211 is "1", the output of the adder 220 is "10,0000,0000", in such case the signed value of the PWM data fed into the latch 231 is not correct. In order to solve this problem, in the present embodiment, before the input data D[11:2] is added to the value of the pulse density modulation signal PDM by the adder 220, the input data D[11:2] is sign extended to an input data with at least 11 bits, so as to generate a PWM data with at least 11 bits. For example, in the case where the input data D[11:2] fed into the adder 220 in the previous case is "01,1111,1111" and the pulse density modulation signal PDM generated by the adder 211 is "1", the input data D[11:2] is sign extended to D[12:2]="001,1111,1111" by the adder 220 first, and its summation is "010,0000,0000", such that the correctness of the signed bit is not impacted.

In view of the foregoing, it is observed **the input data D[11:2] is sign extended to an input data by the first adder of the present invention, thus preventing the incorrect signed value of the PWM data from being fed into the latch 231 due to the data overflow**. Said feature is particularly adapted to the input data having the signed bit used to represent the polarities of the input data. On the contrary, the polarities of the PWM signal PWMout taught by Tanaka are not able to be adjusted through the input signal, and accordingly the issue regarding the data overflow is not resolved by Tanaka. That is to say, the adder 52 disclosed by Tanaka is not capable of resolving the issue with respect to the data overflow which is remedied by the present invention. As such, the adder 220 of the present invention is functionally distinguishable from the adder 52 taught

by Tanaka despite the fact that the two elements are both named the "adder".

For at least the ground furnished above, Applicant respectfully submits that Tanaka does not teach all of the elements recited by the amended claim 1, and therefore claim 1 and its dependent claims 2 and 4-5 are not anticipated by the cited reference of record. Likewise, since the same amendments have been advanced to the independent claim 6, Applicant respectfully submits that the independent claim 6 and claim 8 depending thereupon are novel and patentable over Tanaka.

As well defined in the MPEP 2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Therefore, Applicant respectfully submits Tanaka **does not** anticipate currently amended claim 1 and 6 so that the rejection of claim 1 and 6 should be withdrawn, and the rejections of claims 2, 4, 5, and 8 also should be withdrawn as a matter of law.

Please kindly note that claims 3 and 7 are canceled after the patentable features claimed therein have been incorporated into their respective independent claims 1 and 6. Withdrawal of the 102 rejection of claims 1-2, 4-6, and 8 is accordingly solicited in all sincerity.

Allowable Subject Matter

Claims 4, 5, and 8 remain allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As admitted by the Examiner, Tanaka does not show the PWM including a latch, an absolute value calculator, a counter, a comparator and positive and negative PWM

outputs. Said features are not removed in the proposed amendments submitted herein, and thus the allowability of claims 4, 5, and 8 shall remain.